



NSC

NEURAL SYSTEMS CORPORATION

Trainable Detectors

About NSC Detectors

Reaching New Limits With Trainable Detectors

“A trainable detector first optimally detects a bit stream. Then logic within the detector circuitry detects and corrects errors.”

In 1948 C. Shannon, the founder of Information Theory, published a paper which showed that no more than $C = W \log(1 + \text{SNR})$ bits could be transmitted over a digital communications channel without error, where C is called the channel capacity in bits/sec/Hz, W is the channel bandwidth in Hz, and SNR is the signal-to-noise power ratio. He also proved that codes existed that allowed rates arbitrarily close to C with arbitrarily small error rates

He did not show how to construct these codes, and none were discovered until 1993 when turbo codes were invented that have rates close to C for low SNRs (e.g., 3 db) but not at high SNRs of 15 to 30 db. Commercial digital channels such as DSL, broadband cable and hard disk drive read channels usually operate at SNRs of greater than 15 db.

With partial support from the National Institute of Standards and Technology NSC developed techniques for achieving Shannon channel capacity for communication channels when the SNR is above 15 db, and for hard disk drive channels when it is greater than 20 db. The significance of these developments is that they permit the greatest possible bit rates or densities at these common SNRs. Implementation of the NSC technology will be less complicated than implementing turbo codes.

A trainable detector first optimally detects a bit stream. Then logic within the detector circuitry detects and corrects errors. The Figure is a graph of a hard disk read channel BER for different ratios of energy per bit to noise spectral density (E_b/N_0). The dashed line shows the performance of the standard disk drive detector (called EPR-4). The dotted line shows the performance of the NSC

detector without error correction and the solid line gives the BER after correction. The corrected performance is an improvement of great significance and is very nearly as good as can be done. SCC is reached at a (E_b/N_0) of 14.5 db.

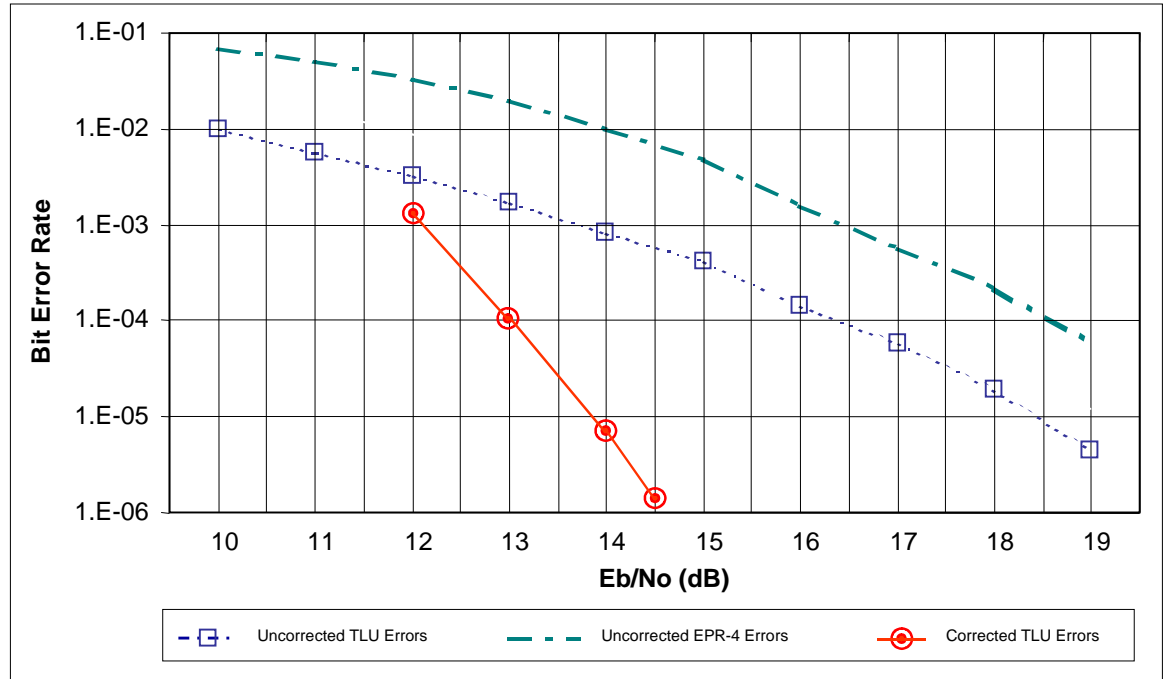


Figure 4. TLU vs EPR-4 Performance at Density 4.25 after Post-Processing
Error correction produces Shannon channel capacity at $E_b/N_0 = 14.5$

The Table is a comparison of error detection simulations with a standard 256 QAM detector at high SNRs, which are typical of cable and DSL channels. A rate of 5.7 bits per sec per Hz is the maximum that can be achieved with 256 QAM at the SNR of 27.5 db. The NSC processing improves this rate by ratio of 1.39. At the SNR of 30.5 db the ratio is 1.93, and at 33.5 it is 2.3 times greater than that of 256 QAM at 27.5 db.

Table 1. Comparison of QPSK and 256 QAM Performance

Mode	SNR (dB)	Bits/Sec/Hz	Uncorrected BER	Corrected BER	%SCC
256 QAM	27.5	5.7	10 ⁻⁸	---	62
QPSK	27.5	7.9	7.2 x 10 ⁻³	10 ⁻⁵	86
QPSK	30.5	11	2.8 x 10 ⁻⁴	< 10 ⁻⁶	98
QPSK	33.5	13.3	2.7 x 10 ⁻⁵	< 10 ⁻⁶	100